An Active SiGe Sub-Harmonic Direct-Conversion Receiver Front-End Design for 5-6 GHz Band Applications

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Abstract — **This paper describes a packaged SiGe RF front-end design for use in the Unlicensed National Information Infrastructure (U-NII) bands. The front-end is based on a sub-harmonic direct-conversion architecture and is composed of an LNA, I and Q x2 sub-harmonic mixers (SHMs), and an LO conditioning chain. The receiver is completely differential and is designed for operation from a 3.3 V supply. Simulated performance shows >25 dB conversion gain, 6.8 dB noise figure (cascode LNA), 0° I/Q phase imbalance, and 39.1 mA total current consumption. To the authors' knowledge, this is the first 5-6 GHz SiGe active sub-harmonic direct-conversion receiver design presented in literature.**

I. Introduction

The demand for low-cost, low-power, wide bandwidth, and highly integrated RF circuitry in the commercial market has made direct-conversion architectures attractive. By eliminating the need for expensive, off-chip image reject and band select filters, and allowing amplification and filtering of the down-converted signal to occur at baseband, direct-conversion offers a solution that not only is highly integrated, but also potentially lower power [1].

Of course, direct-conversion has its own set of issues that must be addressed. First, the translation of the desired RF spectrum to 0 Hz dictates that the down-conversion be done in quadrature to recover the "negative-frequency" portion of the spectrum [1]. This adds an additional level of complexity to the receiver. Direct-conversion receivers are also susceptible to dynamic range limitations that further complicate the architecture's design, primarily due to: second-order distortion, $1/f$ noise, and LO self-mixing [2]. Dynamically changing DC-offsets resulting from either nearby interferers or LO leakage self-mixing can limit the performance of direct-conversion receivers.

This paper presents an RF direct-conversion front-end for 5-6 GHz (U-NII band) applications that is designed with the above issues in mind. By using a differential topology, second-order distortion can be minimized; by designing with SiGe hetero-junction bipolar transistors (HBT), $1/f$ noise is less of a concern than in FET technologies while maintaining compatibility with CMOS circuitry. In addition, by using a sub-harmonic direct-conversion scheme, LO self-mixing can be mitigated. In [3] a GaAs direct-conversion receiver based on a passive sub-harmonic mixer at 5.8 GHz has been reported; active SiGe sub-harmonic mixers have been reported in [2], [4], [5].

The design presented here includes two sub-harmonic mixers for quadrature (I and Q) down-conversion, a differential LNA, and conditioning circuitry to provide the required LO phases to the two mixers. A low-profile MLF package supports the chip, and package and bondwire parasitics are included in the design. The circuit is designed for a supply voltage of 3.3 V. A block diagram of the receiver is shown in Fig. 1.

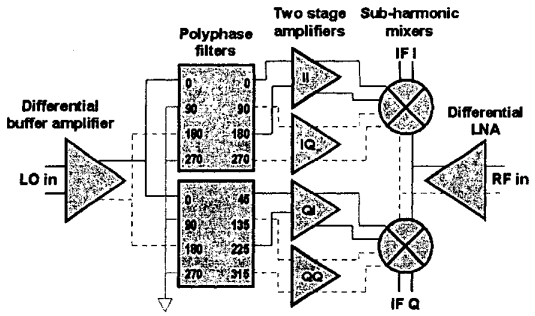

Fig. 1. Block diagram of the receiver front-end.

II. Circuit Topology and Design

Fig. 2 shows a simplified schematic for the x2 sub-harmonic mixer. The design and operation of this circuit is based on a stacked Gilbert-cell topology as described in [2], [5]. The LO signal is applied to the mixer switching stage in quadrature form in order to achieve the second harmonic mixing. The double-stacked transistors operate as an exclusive-OR on the applied quadrature signals, such that the effective LO presented to the transconductance stage is twice the actual LO frequency. The circuit is completely differential so not only are the 0° and 90° phases necessary, but also their compliments at 180° and

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RF-to-baseband down-conversion in direct-conversion is also done in quadrature. Thus another sub-harmonic mixer, and another set of quadrature differential LO signals, with phases at 45°, 135°, 225°, and 315° (denoted as the Q phases), are required. In total, the LO signal is split into eight different phases. The resulting LO components are referred to here as II, IQ, QI, and QQ (see Fig. 1).

With the second stage added to the LO switching core, the sub-harmonic mixer has significantly less voltage headroom than the typical Gilbert-cell mixer. To address this, the RF section is biased in parallel with, and AC coupled to, the LO switching section, as described in [5]. Large resistors are used to load the LO section to reduce the voltage drop to the collector, and to increase overall conversion gain. Resistors are also used to bias this section thus further reducing voltage requirements [5].

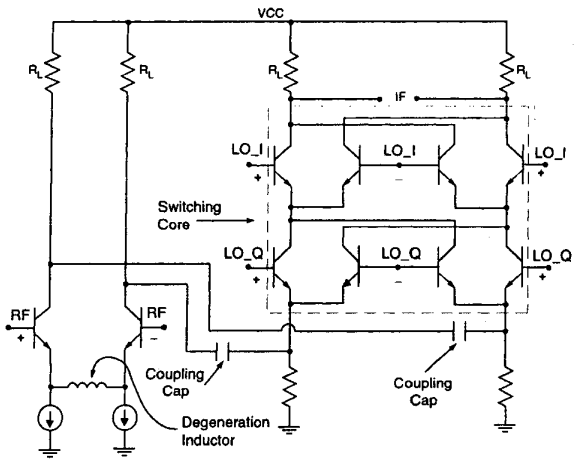

Fig. 2. Schematic of the x2 sub-harmonic mixer core.

A. Polyphase Splitter

Generating the eight different LO phases is done with two polyphase splitters. Each splitter is composed of a combination of R-C poles; a detailed explanation of the basic R-C splitter operation is given in [6]. Analysis of the simple polyphase splitter shows that each R-C pole generates a 45° phase shift. Realizing this, the requisite phases can be generated in a simple manner: an even number of poles will supply the 0°/90°/180°/270° (I) phases; an odd number of poles will provide the 45°/135°/225°/315° (Q) phases.

Fig. 3 shows the schematic of the polyphase splitter. In the top half of the schematic, four poles are used to generate the I phases; in the bottom half, three poles are used to generate the Q phases. Each additional pole will improve the flatness of the filter's amplitude response; however, each additional pole also reduces the amplitude of the LO signal and will require more amplification at the polyphase output for proper operation of the mixer LO switching core. Therefore, a tradeoff exists between the flatness of the splitter's response across the band of interest and the current consumption of the entire LO chain.

In the case of this design, the RF frequency is 5-6 GHz and the LO is RF/2 (2.5-3 GHz). To obtain reasonable flatness while minimizing current consumption, the three and four pole circuits were chosen. The series output capacitors provide a means of centering the polyphase response in the band of interest. A differential buffer-amplifier precedes the polyphase splitter to isolate the filter's input from package parasitics.

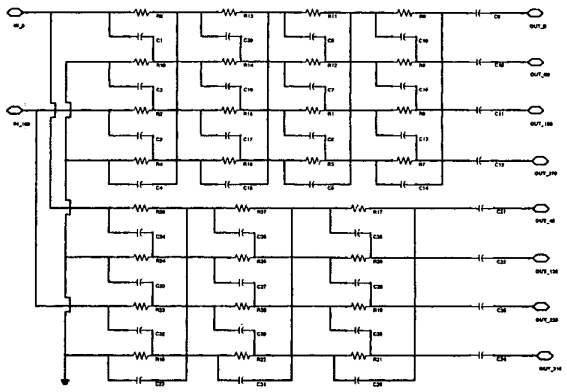

Fig. 3. Simplified polyphase splitter schematic.

B. Two-stage LO Amplifiers

The amplitude of the LO signals applied to the mixer must be large enough to fully turn on/off the double-stacked transistors in the switching core of the mixer. Due to the losses through the polyphase splitter, post-amplification of the LO is required.

Since the number of poles in each filter is different, the required gain of the amplifiers following the polyphase splitters will also be different. To maintain the proper LO signal level to the mixer, two separate two-stage differential amplifiers are designed — one for the receiver I branch and one for the Q.

C. LNA and RF Matching

A schematic of one LNA design is shown in Fig. 4. This LNA includes a cascode differential pair for high input/output isolation, with series input inductors for matching, and inductive collector loading to minimize the overall noise figure and to improve voltage headroom. A second non-cascode design was also implemented, with superior noise figure, but inferior matching/isolation. While both LNA inputs are differential, modifying either

one to include a single-to-differential buffer (e.g. to match to a single-ended band select filter) is straightforward.

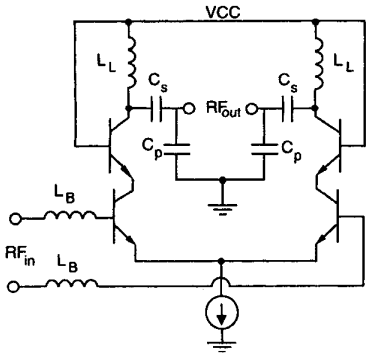

Fig. 4. Simplified schematic of the differential LNA.

The LNA output (RF_{out} in Fig. 4) is directly matched to the input of the I and Q mixers (RF+ and RF- in Fig. 2). The two mixers are in parallel, reducing the differential impedance presented to the LNA. Each mixer input match is controlled by the emitter inductive degeneration; increasing the degeneration improves mixer linearity. However, the parasitic effects associated with on-chip inductors limit the amount of inductance that can be used and hence, the achievable linearity. Because the receiver is designed for direct-conversion, the need to match to an off-chip image reject filter is eliminated and the impedance between the LNA and the mixers can be set independently. The same is true for low-IF applications as image rejection can take place at baseband. For reasonable linearity, a 200Ω differential input impedance for each mixer was chosen, corresponding to a 2.1 nH inductor in each mixer emitter. A simple inter-stage matching network that incorporates the inductive loading of the LNA is used to match the effective 100Ω differential input of the two mixers in parallel to the output of the LNA.

II. Simulated Results

The receiver designs are implemented in IBM's 5HP SiGe technology. Using the well-defined models for the components within this technology, simulated results can be used to predict the overall performance. Fig. 5 shows the overall conversion gain and noise figure of the cascode LNA receiver I branch vs. LO power at an IF of 10 MHz. A non-zero IF is chosen to guarantee simulator convergence (also relevant for low-IF). The non-cascode LNA receiver has a similar characteristic, but exhibits a maximum gain of 21.8 dB and a minimum noise figure of 4.9 dB. Fig. 6 shows the I/Q phase balance as a function of LO power for the cascode LNA receiver. From this graph, 0° phase error is achieved at an LO power of –2 dBm with ±1° error over the –4 to 0 dBm LO power range. The non-cascode LNA receiver has similar performance.

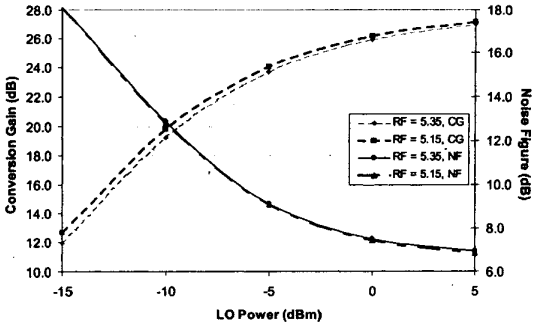

Fig. 5. Simulated results for overall conversion gain and noise figure of the I-channel (RF → IF-I). Here, the RF is set to 5.15 and 5.35 GHz with the LO set to 2.57 and 2.67 GHz, respectively, representing the top and bottom ends of the lower two U-NII bands. Q-channel results are similar.

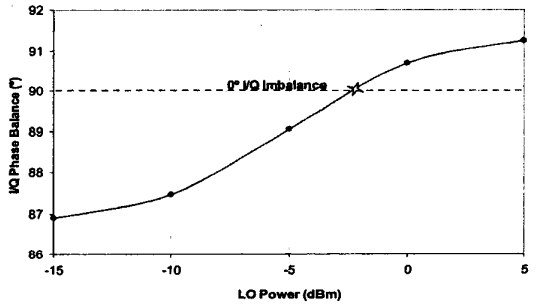

Fig. 6. Simulated phase balance between the IF outputs of the I and Q mixers at f_{RF} = 5.15 GHz and f_{LO} = 2.57 GHz. The desired phase difference of 90° is noted.

From non-linear simulations, the estimated IIP_3 for the receiver is around 0 dBm and the sensitivity is estimated to be -102 dBm, assuming a 5 MHz bandwidth. The total simulated current consumption is 39.1 mA — 5 mA for each mixer, 6.6 mA for the LNA, and 22.5 mA for the LO conditioning chain.

III. Measured Results

Fig. 7 shows the measured conversion gain of a single prototype sub-harmonic mixer as a function of LO power at 5.25 GHz, the center frequency of the lower U-NII band [5]. The measured flatness of the conversion gain vs. frequency was 9 dB ± 0.2 dB for the lower two U-NII bands. These results show the feasibility of the sub-harmonic

mixer concept that the direct-conversion architecture described above is based upon.

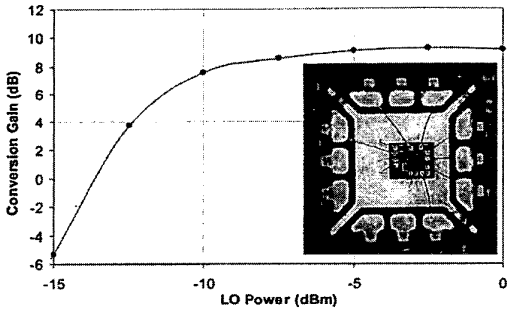

Fig. 7. Measurement of single sub-harmonic mixer conversion gain vs. LO power at an RF frequency of 5.25 GHz. Inset: Photograph of single packaged prototype sub-harmonic mixer.

IV. Layout and Packaging

The chip is to be packaged in a low-profile MLF 32-pin 5 mm x 5 mm package. The bond wires and package parasitics have a significant impact on the performance of the receiver. For the prototype sub-harmonic mixer in Section III, the bond wires were modeled as described in [7]. For the direct-conversion receiver, parasitics were determined using EM simulations, as accurate modeling is critical to the RF input match and the output I/Q phase balance. Notably, the bond wire inductance can be beneficial by reducing the total on-chip inductance used for input matching.

Fig. 8 shows the layout of the full direct-conversion receiver. The RF is applied at the right-side of the chip, the LO at the left, and the IF is taken from the top and bottom. "Guard rings," consisting of rows of substrate contacts placed between deep-trench, are used to enhance isolation between the various sub-circuits, with particular attention to separating the RF/LO sections and the I/Q sections. The LO conditioning circuitry is carefully laid out to guarantee that parasitics do not interfere with the phase balance. This entails "wrapping" the signal carrying lines at fixed distances to make sure the parasitics between lines are identical.

V. Conclusion

The receiver described above is currently in fabrication. Complete performance results for the full direct-conversion receiver will be presented at the symposium. To the authors' knowledge, this is the first 5-6 GHz SiGe *active sub-harmonic* direct conversion receiver design presented in the literature.

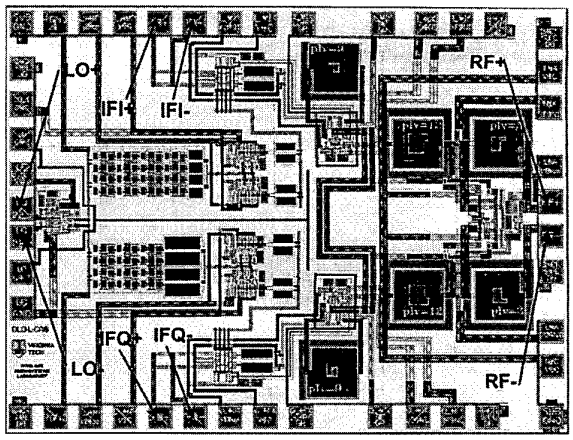

Fig. 8. Layout of direct-conversion receiver currently in fabrication. Chip area is ~2.3 mm x 1.8 mm.

Acknowledgement

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